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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,642	08/30/2001	Giovanni Santin	400.070US01	9387

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LEFFERT JAY & POLGLAZE, P.A.
P.O. BOX 581009
MINNEAPOLIS, MN 55458-1009

EXAMINER	
NGUYEN, VIET Q	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,642	SANTIN, GIOVANNI	
	Examiner	Art Unit	
	Viet Q Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *THREE* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Application filed on 9/30/2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-96* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-96* is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/30/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-96** are present for examination.

Claim Rejections - 35 USC § 103

1. Claims **1-13** rejected under 35 U.S.C. 103(a) as being unpatentable over **Wright et al (6,550,026).**

Wright et al (see Fig.3) shows a testing circuit for compression testing, which includes a first logic circuit (NOR gate 210) for receiving data signals corresponding to a given location (odd/even locations) of each first word of an output page (from an array) of the memory device (array 11A, Fig.1) and for providing first output signals indicative of whether each data signal (DR) from these given bit locations (even/odd) has a first logic level (0 or 1) or not; a second logic circuit (NAND gate 208) for receiving data signals corresponding to a given bit location (odd/even locations) of each word of an output page (from an array) of the memory device (array 11A, Fig.1) and for providing second output signals indicative of whether each data signal (DR) from these given bit locations (even/odd) has a first logic level (0 or 1) or not. For example, col.8 (lines 14-19) specifically stated that "***the NAND and NOR gates 208 and 210 both output a high value if all of their inputs are low, and alternatively both output a low value if all inputs are high***." Fig.3 also shows the use of a third logic circuit (exclusive OR gate 212) for comparing the output signals from gates (208 and 210) and for providing third output signals indicative whether or not each data

signal (DR) has the same logic or not. Co.8 (lines 24-34) also mentions the use of additional circuits for comparing the third output signals from gate 212 to thereby compare the corresponding bit locations from the first data word with a third data word. Thus, it would have been obvious to one skilled in this art that Wright et al also suggest the compression testing for a same given bit location across different words (of a memory array) altogether at the same time.

In regard to other claims, Fig.3 also shows that first logic circuit is a NOR gate (210) and the second logic circuit is a NAND gate for receiving as claimed. Both gates receiving a plurality of data signals corresponding top a given bit location of each data word, and both seem to have two logic levels (e.g., low or high). Further, the third logic circuit (212) is also an XOR gate as recited. However, other obvious design and/or alternative gating arrangement are considered as expedient choice to one skilled in this art in so far as the same output result or logical equivalent value is concerned.

2. Other claims contain allowable subject matter over prior arts of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2818

V. Nguyen
10/15/2004